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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/667,164	Applicant(s) BALLACHINO, WILLIAM E.	
	Examiner Chat C. Do	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Uya (U.S. 4,682,303).

Re claim 1, Uya discloses in Figure 2 an M-bit adder (M = 26) capable of receiving a first M-bit argument (A0-A25), a second M-bit argument (B0-B25), and a carry-in "Ci" (C4, C8, C13, C19, and C26) bit comprising: M adder cells arranged in R rows (P1, P2, P3, P4, and P5), wherein a least significant adder cell in a first one of rows of adder cells (P2) receives a first data bit, Ax (A4), from first M-bit argument (A) and a first data bit, Bx (B4), from second M-bit argument (B), and generates a first conditional carry-out bit, Cx(1) (C5 in Figure 3), and a second conditional carry-out bit, Cx(0) (C5 in Figure 4), wherein CH0 bit is calculated assuming a row carry-out bit from a second row of adder cells preceding first row is a 1 and CL0 bit is calculated assuming row carry-out bit from second row is a 0 (Figure 3 and 4).

Re claim 2, Uya further discloses in Figure 2 least significant adder cell generates a first conditional sum bit (S4 in Figure 3), and a second conditional sum bit (S4 in Figure 4).

Re claim 3, Uya further discloses in Figure 2 Sx(1) bit is calculated assuming row carry-out bit from second row is a 1 (65) and Sx(0) bit is calculated assuming 4 row carry-out bit from second row is a 0 (70).

Re claim 4, Uya further discloses in Figure 2 row carry-out bit selects one of Sx(1) bit and Sx(0) bit to be output by least significant adder cell (32).

Re claim 5, Uya further discloses in Figure 2 first row of adder cells further comprises a second adder cell (adder for adding A5 and B5) coupled to least significant adder cell, wherein second adder cell receives a second data bit (A5), from first M-bit argument and a second data bit (B5), from second M-bit argument, and receives from least significant adder cell (output of 67) bit and (output of 72) bit.

Re claim 6, Uya further discloses in Figure 3 second adder cell (adder for adding A5 and B5) generates a first conditional carry-out bit (C6 in Figure 3), wherein Cx1(1) bit is generated from A5 data bit, B5 data bit, and CH0 bit (C5 from previous adder) from least significant adder cell (right portion of 21).

Re claim 7, Uya further discloses in Figure 2 second adder cell (adder for adding A5 and B5) generates a second conditional carry-out bit (output of 64' in Figure 4), wherein Cx1(0) bit is generated from A5 data bit, B5 data bit, and CL0 bit (C5 from previous adder in Figure 4) from least significant adder cell (right portion of 20).

Re claim 8, Uya further discloses in Figures 1-4 second adder cell (adder for adding A5 and B5) generates a first conditional sum bit S1 (S5 in Figure 3), wherein S1 bit is generated from A5 data bit, B5 data bit, and CH0 bit from least significant adder cell.

Re claim 9, Uya further discloses in Figures 1-4 second adder cell (adder for adding A5 and B5) generates a second conditional sum bit, wherein S1 (S5 in Figure 4) bit is generated from A5 data bit, B5 data bit, and CL0 bit from least significant adder cell.

Re claim 10, Uya further discloses in Figures 1-4 row carry-out bit selects one of Sl(1) bit and Sl(0) bit to be output by second adder cell (24 and 25 in Figure 2).

Re claim 11, Uya further discloses first row of adder cells contains N adder cells and second row of adder cells preceding first row contains less than N adder cells (P3, P4, and P5 wherein P3 has 5 adder cells, P4 has 6 adder cells, and P5 has 5 adder cells).

Re claim 12, it is a processor claim of claim 1. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 13, it is a processor claim of claim 2. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 14, it is a processor claim of claim 3. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 15, it is a processor claim of claim 4. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 16, it is a processor claim of claim 5. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 17, it is a processor claim of claim 6. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 18, it is a processor claim of claim 7. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 19, it is a processor claim of claim 8. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 20, it is a processor claim of claim 9. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 21, it is a processor claim of claim 10. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 22, it is a processor claim of claim 11. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 23, it is a method claim of claim 1. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 1.

3. Claims 1-10, 12-21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Ranjan (U.S. 5,852,568).

Re claim 1, Ranjan discloses in Figures 1, 3, and 4 an M-bit adder (M = 32) capable of receiving a first M-bit argument (X0-X31), a second M-bit argument (Y0-Y31), and a carry-in "Ci" (155) bit comprising: M adder cells arranged in R rows (As seen in Figure 1 first row is 102a, second row is 102b...), wherein a least significant adder cell in a first one of rows of adder cells (102a) receives a first data bit, Ax (X0), from first M-bit argument (X) and a first data bit, Bx (Y0), from second M-bit argument (Y), and generates a first conditional carry-out bit, Cx(1) (CH0), and a second conditional

carry-out bit, Cx(0) (CL0), wherein CH0 bit is calculated assuming a row carry-out bit from a second row of adder cells preceding first row is a 1 and CL0 bit is calculated assuming row carry-out bit from second row is a 0 (col. 2 lines 5-13).

Re claim 2, Ranjan further discloses in Figures 1-4 least significant adder cell generates a first conditional sum bit (310a), and a second conditional sum bit (313a).

Re claim 3, Ranjan further discloses in Figures 1-4 Sx(1) bit is calculated assuming row carry-out bit from second row is a 1 (363a) and S,(0) bit is calculated assuming 4 row carry-out bit from second row is a 0 (360a).

Re claim 4, Ranjan further discloses in Figures 1-4 row carry-out bit selects one of Sx(1) bit and Sx(0) bit to be output by least significant adder cell (155).

Re claim 5, Ranjan further discloses in Figures 1-4 first row of adder cells further comprises a second adder cell (395b in Figure 3 and 450b in Figure 4) coupled to least significant adder cell, wherein second adder cell (395b in Figure 3 and 450b in Figure 4) receives a second data bit (X1), from first M-bit argument and a second data bit (Y1), from second M-bit argument, and receives from least significant adder cell (CH0 into 363b in Figure 3) bit and (CL0 into 360b in Figure 3) bit.

Re claim 6, Ranjan further discloses in Figures 1-4 second adder cell (395b in Figure 3 and 450b in Figure 4) generates a first conditional carry-out bit (260b), wherein Cx1(1) bit is generated from X1 data bit, Y1 data bit, and CH0 bit from least significant adder cell (by 460a).

Re claim 7, Ranjan further discloses in Figures 1-4 second adder cell (395b in Figure 3 and 450b in Figure 4) generates a second conditional carry-out bit (265b),

wherein Cxl(0) bit is generated from X1 data bit, Y1 data bit, and CL0 bit from least significant adder cell (by 465a).

Re claim 8, Ranjan further discloses in Figures 1-4 second adder cell (395b in Figure 3 and 450b in Figure 4) generates a first conditional sum bit S1 (313b), wherein S1 bit is generated from X1 data bit, Y1 data bit, and CH0 bit from least significant adder cell (SH1).

Re claim 9, Ranjan further discloses in Figures 1-4 second adder cell generates a second conditional sum bit, wherein S1 (310b) bit is generated from X1 data bit, Y1 data bit, and CL0 (360b) bit from least significant adder cell (from previous cell).

Re claim 10, Ranjan further discloses in Figures 1-4 row carry-out bit selects one of Sl(1) bit and Sl(0) bit to be output by second adder cell (155 in Figure 1).

Re claim 12, it is a processor claim of claim 1. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 13, it is a processor claim of claim 2. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 14, it is a processor claim of claim 3. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 15, it is a processor claim of claim 4. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 16, it is a processor claim of claim 5. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 17, it is a processor claim of claim 6. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 18, it is a processor claim of claim 7. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 19, it is a processor claim of claim 8. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 20, it is a processor claim of claim 9. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 21, it is a processor claim of claim 10. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 23, it is a method claim of claim 1. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Ranjan (U.S. 5,852,568) in view of Ware (U.S. 4,623,982).

Re claim 11, Ranjan does not disclose first row of adder cells contains N adder cells and second row of adder cells preceding first row contains less than N adder cells.

However, Ware discloses in Figure 3B a structure arrangement in conditional adder wherein the first row of adder cells contains N adder cells and second row of adder cells preceding first row contains less than N adder cells. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to slightly arrange the conditional adder cells as disclosed in Ware's invention into Ranjan's invention because it would enable to substantially increase the system performance by optimizing the overall delay.

Re claim 22, it is a processor claim of claim 11. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 11.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,396,445 to Lal discloses a binary carry-select adder.

b. U.S. Patent No. 5,732,008 to Abu-Khater et al. disclose a low-power high performance adder.

c. U.S. Patent No. 5,579,254 to Kumar et al. disclose a fast static CMOS adder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

June 30, 2003

CHUONG DINH NGO
PRIMARY EXAMINER